UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/467,992	12/20/1999	LEONARD FORBES	303.389US2	3099

21186 7590 06/01/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/467,992	FORBES ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-19,22,23,25-27,29 and 31-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-19,22,23,25-27,29 and 31-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/1/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the transistor including a first source/drain region, a body region and a second source/drain region, that are vertically aligned and **a trench capacitor ... coupled to the first source/drain region**, and **a second plate of polycrystalline material ... that is coupled to a first plate** (i.e. claim 17) must be shown or the feature(s) canceled from the claim(s).

Also, the transistor further including a gate adjacent to the body region and the gate being vertically aligned with the second plate must be shown. FIG. 1 does not show a gate. FIG. 6 is not show a transistor that is vertically aligned. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "104" has been used to designate both access transistor and pillar. See page 6, line 21 and page 6, line 14. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. The amendments filed 7/21/04 and 10/14/04 are objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the transistor including a first source/drain region, a body region and a second source/drain region, that are vertically aligned and a trench capacitor ... coupled to the first source/drain region, and a second plate of polycrystalline material ... that is coupled to a first plate and the transistor further including a gate adjacent to the body region and the gate being vertically aligned with the second plate.

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 17 thru 19, 31, 32, 37, 46, and 48 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not describe a transistor including a first source/drain region, a body region and a second source/drain region, that are vertically aligned **and** wherein the trench

capacitor ... coupled to the first source/drain region, and a second plate of polycrystalline material ... that is coupled to a first plate (claim 17).

The specification does not describe the transistor further including a gate adjacent to the body region and the gate being **vertically** aligned with the second plate (claim 17).

In claims 19 and 32, the specification does not describe the first plate comprising a heavily doped p-type silicon substrate.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Insofar as definite, claims 17 thru 19, 22, 23, 25, 31 thru 34, 37 thru 39, 41 thru 46, 48, and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh 4,920,389 in view of Kanetaki et al. 4,906,590. Itoh discloses (see, for example, FIG_ 8(k)) a memory cell array structure comprising memory cells wherein an individual memory cell comprises bit lines 222, word lines 234, a low electric resistance region (first source/drain region) 232, high electric resistance semiconductor layer (body region) 204, low electric resistance semiconductor layer (second source/drain region) 202, highly electroconductive layer (second plate) 216 and gate 234. In column 13, lines 18-32, Itoh discloses the low electric resistance semiconductor layer 202 serving as a first electrode (first plate) of a capacitor as well as a source region. In column 10, lines 31-41, Itoh discloses the highly electroconductive layer comprising polycrystalline

silicon. Itoh does not disclose an etch-roughened surface. However, Kanetaki discloses (see, for example, FIG. 2) a trench capacitor containing two plurality of hollows (roughened surfaces). In column 1, lines 11- *, Kanetaki states that the plurality of hollows increases the electrode area without increasing the planar area. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to include the plurality of hollows (roughened surfaces) in Itoh's invention in order to increase the electrode area without increasing the planar area.

8. Claims 26, 27, 29, 35, 36, 40, 47, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh '389 in view of Kanetaki et al. '590 as applied to claims 17-19, 22, 23, 25, 31 thru 34, 37-39, 41 thru 46, 48, and 49 above, and further in view of Wahlstrom 5,396,452. Itoh in view of Kanetaki does not disclose a row decoder and column decoder so as to selectively access the cells of an array. However, Wahlstrom discloses (see, for example, FIG. 2) a dynamic random access memory comprising memory cells arranged in an array wherein word lines (WL) are arranged orthogonal to bit lines (BL). In FIG. 1, Wahlstrom shows a row decoder and a column decoder which access the memory cells according to the row and column addresses applied. It would have been obvious to one of ordinary skill in the art at the time of invention to have a column and row decoder in order to form a memory cell array wherein the individual memory cells may be accessed easily.

Response to Arguments

9. Applicant's arguments with respect to claims 17-19, 22, 23, 25-27, 29, 31-50 have been considered but are moot in view of the new ground(s) of rejection.

Regarding the Drawing Objection and 112 rejection, FIG. 1 does not show the trench capacitor 120, 122, 110 coupled to the first source/drain region 106. The first source 106 is only coupled to a bit line 118. FIG. 1 does not show a gate.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tom Thomas

Eugene Lee
May 22, 2004

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800